Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claim 1, and add new claims 42-86, as follows:

Listing of Claims:

1-41. (Cancelled)

42. (New) A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

in response to a start signal, generating a plurality of counting clock signals, one of the counting clock signals designated a reference counting clock signal and the remaining counting clock signals having a delay relative to the reference counting clock signal;

in response to the start signal, counting a number of clock cycles of the reference counting clock signal until a transition of the applied clock signal subsequent to the start signal;

counting the same number of clock cycles responsive to a transition of the reference counting clock signal subsequent to the transition of the applied clock signal;

determining a fine delay that is based on the states of the counting clock signals at the time of the transition of the applied clock signal; and

generating the delayed clock signal having a delay relative to the applied clock signal that is equal to the time for counting the number of clock cycles in response to the start signal, for counting the same number of clock cycles responsive to the transition of the reference counting clock signal, and the fine delay.

43. (New) The method of claim 42 wherein counting the number of clock cycles in response to the start signal comprises incrementing a delay count responsive to the counting clock signal in response to an Nth transition of the applied clock signal and terminating the counting responsive to an N+1th transition of the applied clock signal.

44. (New) The method of claim 43 wherein counting the same number of clock cycles responsive to a transition of the reference counting clock signal comprises decrementing the delay count responsive to the counting clock signal until delay count is equal to the value at the time counting was initiated in response to the start signal.

45. (New) The method of claim 42, further storing states of the counting clock signals and calculating a digital-to-time fine delay from the stored states of the counting clock signals according to a first methodology responsive to a selected one of the counting clock signals having a first logic state.

46. (New) The method of claim 45 wherein calculating the digital-to-time fine delay from the stored states of the counting clock signals comprises calculating the fine delay according to a second methodology responsive to a selected one of the counting clock signals having a second logic state.

47. (New) The method of claim 42, further comprising storing the instantaneous states of the counting clock signals, and thereafter performing an XOR operation on adjacent pairs of clock signals to generate a plurality of fine delay control signals, with the fine delay control signal having a false value indicating the location of the reference counting clock signal edge at the point in time when the counting of the number of clock cycles ceases.

48. (New) A method for generating a delayed clock signal having a delay relative to an applied clock signal, the method comprising:

generating a plurality of oscillator clock signals, each oscillator clock signal having a frequency that is greater than the applied clock signal, with one oscillator clock signal being designated a reference oscillator clock signal and each oscillator clock signal having a delay relative to the reference oscillator clock signal;

measuring a coarse delay time in response to transitions of the reference oscillator clock signal;

storing the state of the oscillator clock signals at a first time;

replaying the coarse delay time;

calculating a fine delay time from the states of the oscillator clock signals at the first time; and

generating the delayed clock signal having a delay relative to the applied clock signal that is given by the sum of the coarse delay time plus the replayed coarse delay time plus the fine delay time.

49. (New) The method of claim 48 wherein measuring the coarse delay time comprises timing a digital-to-time coarse delay time in response to transitions of the reference oscillator clock signal after the first time.

50. (New) The method of claim 48 wherein storing the state of the oscillator clock signals at a first time comprises storing the instantaneous states of the oscillator clock signals, and thereafter performing an XOR operation on adjacent pairs of clock signals to generate a plurality of fine delay control signals, with the fine delay control signal having a false value indicating the location of the reference oscillator clock signal edge at the first time.

51. (New) The method of claim 48 wherein a first circuit generates the plurality of oscillator clocks signals, times the coarse delay time, and calculates the fine delay time, and wherein a second circuit replays the coarse delay time and generates the delayed clock signal.

52. (New) The method of claim 51 wherein the first and second circuits are different circuits.

53. (New) A clock synchronizing circuit, comprising:

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal in response to receiving a model delay signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a delay circuit coupled to the ring oscillator and having an input to which an input clock signal is applied and operable to generate the model delay signal in response to the input clock signal having a delay relative to the input clock signal;

a delay measuring circuit having a first measuring circuit coupled to the ring oscillator to receive the oscillator clock signal, the first measuring circuit operable to generate a first digital measurement signal indicative of a count value of the number of cycles of the oscillator clock signal between the model delay signal and the input clock signal, and further having a second measuring circuit coupled to the ring oscillator to receive the tap clock signals and operable to latch the tap clock signals responsive to the input clock signal to generate a second digital measurement signal; and

at least one replay circuit having a first replay circuit coupled to the ring oscillator, the delay circuit, and the first measuring circuit, and further having a second replay circuit coupled to the ring oscillator, the second measuring circuit, and the first replay circuit, the first replay circuit operable to store the first digital measurement signal and further operable to generate a cycle count based on the oscillator clock signal and generate a first replay signal responsive to the cycle count being equal to the stored digital delay measurement signal, and the second replay circuit operable to generate a delayed clock signal responsive to the first replay signal and a first clock edge of one of the tap clock signals selected in accordance with the second measurement signal.

54. (New) The clock synchronizing circuit of claim 53 wherein the second replay circuit comprises:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock

signal on an output responsive to a plurality of input selection signals, the tap clock signal on the output corresponding to the delayed clock signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the input clock signal and to generate a plurality of delay signals responsive to the latched tap clock signals; and

a delay transform circuit coupled to receive the first digital measurement signal and coupled to the latch and compare circuit and the multiplexer, the delay transform circuit operable in response to the delay signals to select a respective input selection signal and to activate the selected input selection signal responsive to the first replay signal going active.

55. (New) The clock synchronizing circuit of claim 54 wherein the multiplexer comprises a plurality of transmission gates.

56. (New) The clock synchronizing circuit of claim 54 wherein the ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding delay signal.

57. (New) The clock synchronizing circuit of claim 56 wherein the delay transform circuit operates in a first mode responsive to a selected one of the tap clock signals T1-TN having a first logic state.

58. (New) The clock synchronizing circuit of claim 57 wherein the delay transform circuit operates in a second mode responsive to a selected one of the tap clock signals T1-TN having a second logic state.

59. (New) The clock synchronizing circuit of claim 53 wherein the first measuring circuit and the first replay circuit share a circuit comprising:

an up/down counter coupled to receive the input clock signal and the model delay signal, and coupled to the ring oscillator to receive the oscillator clock signal, the up/down counter operable responsive to a transition of the model delay signal to increment the count value from a reference count value responsive to the oscillator clock signal, and operable responsive to a transition of the input clock signal to decrement the count value responsive to the oscillator clock signal; and

a comparator coupled to the up/down counter, the comparator activating the first digital measurement signal responsive to the count value being equal to the reference count value.

60. (New) The clock synchronizing circuit of claim 53 wherein the at least one replay circuit comprises first, second, third, and fourth replay circuits coupled to the measuring circuit.

61. (New) A clock synchronizing circuit for generating a delayed clock signal in response to an input clock signal, the synchronizing circuit comprising:

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal in response to receiving a ring oscillator start signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay measuring circuit coupled to the ring oscillator to receive the oscillator clock signal, the coarse delay measuring circuit operable to generate a coarse digital delay measurement signal indicative of a count value of the oscillator clock signal between the ring oscillator start signal and the input clock signal;

a fine delay measuring circuit coupled to the ring oscillator to receive the tap clock signals and operable to latch the tap clock signals responsive to the input clock signal to generate a fine digital delay measurement signal;

a coarse delay replay circuit coupled to the ring oscillator and coarse delay measuring circuit, the coarse delay replay circuit operable to store the coarse digital delay measurement signal and further operable to generate a cycle count based on the oscillator clock signal and generate a coarse delay replay signal responsive to the cycle count being equal to the stored digital delay measurement signal,

a fine delay replay circuit coupled to the ring oscillator, the fine delay measuring circuit, and the coarse delay replay circuit, the fine delay replay circuit operable to generate a fine delay replay signal responsive to the coarse delay replay signal and a first clock edge of one of the tap clock signals selected in accordance with the fine delay measurement signal; and

an output circuit coupled to the coarse and fine delay replay circuits and operable to generate the delayed clock signal responsive to the coarse delay replay signal and the fine delay replay signal.

62. (New) The clock synchronizing circuit of claim 61 wherein the output circuit comprises an AND gate.

63. (New) The clock synchronizing circuit of claim 61 wherein the coarse delay measuring circuit comprises a counter circuit coupled to receive the ring oscillator start signal and coupled to the ring oscillator to receive the oscillator clock signal, the counter circuit operable responsive to a transition of the oscillator start signal to increment the count value from a reference count value responsive to the oscillator clock signal.

64. (New) The clock synchronizing circuit of claim 61 wherein the coarse delay replay circuit comprises a counter circuit coupled to receive the input clock signal and coupled to the ring oscillator to receive the oscillator clock signal, the counter circuit operable responsive to a transition of the input clock signal to decrement the count value responsive to the oscillator clock signal.

65. (New) The clock synchronizing circuit of claim 61 wherein the fine delay measuring circuit and the fine delay replay circuit share a fine delay circuit comprising:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock signal on an output responsive to a plurality of input selection signals, with the tap clock signal on the output corresponding to the fine delay replay signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the input clock signal and to generate a plurality of fine delay signals responsive to the latched tap clock signals; and

a fine delay transform circuit coupled to receive the coarse delay enable signal and coupled to the latch and compare circuit and the multiplexer, the fine delay transform circuit operable in response to the fine delay signals to select a respective input selection signal and to activate the selected input selection signal responsive to the coarse delay replay signal going active.

66. (New) The clock synchronizing circuit of claim 65 wherein the multiplexer comprises a plurality of transmission gates.

67. (New) The clock synchronizing circuit of claim 65 wherein the ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding fine delay signal.

68. (New) The clock synchronizing circuit of claim 67 wherein the fine delay transform circuit operates in a first mode responsive to a selected one of the tap clock signals T1-TN having a first logic state.

69. (New) The clock synchronizing circuit of claim 68 wherein the fine delay transform circuit operates in a second mode responsive to a selected one of the tap clock signals T1-TN having a second logic state.

70. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a clock synchronizing circuit coupled to at least the control circuit and adapted to receive an input clock signal, the clock synchronizing circuit operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the clock synchronizing circuit comprising,

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal in response to receiving a model delay signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a delay circuit coupled to the ring oscillator and having an input to which an input clock signal is applied and operable to generate the model delay signal in response to the input clock signal having a delay relative to the input clock signal;

a delay measuring circuit having a first measuring circuit coupled to the ring oscillator to receive the oscillator clock signal, the first measuring circuit operable to generate a first digital measurement signal indicative of a count value of the number of cycles of the oscillator clock signal between the model delay signal and the input clock signal, and further having a second measuring circuit coupled to the ring oscillator to receive the tap clock signals

and operable to latch the tap clock signals responsive to the input clock signal to generate a second digital measurement signal; and

at least one replay circuit having a first replay circuit coupled to the ring oscillator, the delay circuit, and the first measuring circuit, and further having a second replay circuit coupled to the ring oscillator, the second measuring circuit, and the first replay circuit, the first replay circuit operable to store the first digital measurement signal and further operable to generate a cycle count based on the oscillator clock signal and generate a first replay signal responsive to the cycle count being equal to the stored digital delay measurement signal, and the second replay circuit operable to generate a delayed clock signal responsive to the first replay signal and a first clock edge of one of the tap clock signals selected in accordance with the second measurement signal.

71. (New) The memory device of claim 70 wherein the second replay circuit of the clock synchronizing circuit comprises:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock signal on an output responsive to a plurality of input selection signals, the tap clock signal on the output corresponding to the delayed clock signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the input clock signal and to generate a plurality of delay signals responsive to the latched tap clock signals; and

a delay transform circuit coupled to receive the first digital measurement signal and coupled to the latch and compare circuit and the multiplexer, the delay transform circuit operable in response to the delay signals to select a respective input selection signal and to activate the selected input selection signal responsive to the first replay signal going active.

72. (New) The memory device of claim 71 wherein the multiplexer comprises a plurality of transmission gates.

73. (New) The memory device of claim 71 wherein the ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding delay signal.

74. (New) The memory device of claim 73 wherein the delay transform circuit operates in a first mode responsive to a selected one of the tap clock signals T1-TN having a first logic state.

75. (New) The memory device of claim 74 wherein the delay transform circuit operates in a second mode responsive to a selected one of the tap clock signals T1-TN having a second logic state.

76. (New) The memory device of claim 70 wherein the first measuring circuit and the first replay circuit of the clock synchronizing circuit share a circuit comprising:

an up/down counter coupled to receive the input clock signal and the model delay signal, and coupled to the ring oscillator to receive the oscillator clock signal, the up/down counter operable responsive to a transition of the model delay signal to increment the count value from a reference count value responsive to the oscillator clock signal, and operable responsive to a transition of the input clock signal to decrement the count value responsive to the oscillator clock signal; and

a comparator coupled to the up/down counter, the comparator activating the first digital measurement signal responsive to the count value being equal to the reference count value.

77. (New) The memory device of claim 70 wherein the at least one replay circuit of the clock synchronizing circuit comprises first, second, third, and fourth replay circuits coupled to the measuring circuit.

78. (New) A memory device, comprising:

an address bus;

a control bus;

a data bus;

an address decoder coupled to the address bus;

a read/write circuit coupled to the data bus;

a control circuit coupled to the control bus;

a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; and

a clock synchronizing circuit coupled to at least the control circuit and adapted to receive an input clock signal, the clock synchronizing circuit operable to generate a delayed clock signal and the control circuit generating control signals in response to the delayed clock signal, the clock synchronizing circuit comprising,

a ring oscillator operable to generate a plurality of tap clock signals with one tap clock signal being designated an oscillator clock signal in response to receiving a ring oscillator start signal, each tap clock signal having a respective delay relative to the oscillator clock signal;

a coarse delay measuring circuit coupled to the ring oscillator to receive the oscillator clock signal, the coarse delay measuring circuit operable to generate a coarse digital delay measurement signal indicative of a count value of the oscillator clock signal between the ring oscillator start signal and the input clock signal;

a fine delay measuring circuit coupled to the ring oscillator to receive the tap clock signals and operable to latch the tap clock signals responsive to the input clock signal to generate a fine digital delay measurement signal;

a coarse delay replay circuit coupled to the ring oscillator and coarse delay measuring circuit, the coarse delay replay circuit operable to store the coarse digital delay measurement signal and further operable to generate a cycle count based on the oscillator clock signal and generate a coarse delay replay signal responsive to the cycle count being equal to the stored digital delay measurement signal,

a fine delay replay circuit coupled to the ring oscillator, the fine delay measuring circuit, and the coarse delay replay circuit, the fine delay replay circuit operable to generate a fine delay replay signal responsive to the coarse delay replay signal and a first clock edge of one of the tap clock signals selected in accordance with the fine delay measurement signal; and

an output circuit coupled to the coarse and fine delay replay circuits and operable to generate the delayed clock signal responsive to the coarse delay replay signal and the fine delay replay signal.

79. (New) The memory device of claim 78 wherein the output circuit of the clock synchronizing circuit comprises an AND gate.

80. (New) The memory device of claim 78 wherein the coarse delay measuring circuit of the clock synchronizing circuit comprises a counter circuit coupled to receive the ring oscillator start signal and coupled to the ring oscillator to receive the oscillator clock signal, the counter circuit operable responsive to a transition of the oscillator start signal to increment the count value from a reference count value responsive to the oscillator clock signal.

81. (New) The memory device of claim 78 wherein the coarse delay replay circuit of the clock synchronizing circuit comprises a counter circuit coupled to receive the input clock signal and coupled to the ring oscillator to receive the oscillator clock signal, the counter circuit operable responsive to a transition of the input clock signal to decrement the count value responsive to the oscillator clock signal.

82. (New) The memory device of claim 78 wherein the fine delay measuring circuit and the fine delay replay circuit of the clock synchronizing circuit share a fine delay circuit comprising:

a multiplexer having a plurality of inputs coupled to the ring oscillator, each input receiving a respective tap clock signal, the multiplexer operable to provide a respective tap clock signal on an output responsive to a plurality of input selection signals, with the tap clock signal on the output corresponding to the fine delay replay signal;

a latch and compare circuit coupled to the ring oscillator, the latch and compare circuit operable to latch the tap clock signals responsive to the input clock signal and to generate a plurality of fine delay signals responsive to the latched tap clock signals; and

a fine delay transform circuit coupled to receive the coarse delay enable signal and coupled to the latch and compare circuit and the multiplexer, the fine delay transform circuit operable in response to the fine delay signals to select a respective input selection signal and to activate the selected input selection signal responsive to the coarse delay replay signal going active.

83. (New) The memory device of claim 82 wherein the multiplexer comprises a plurality of transmission gates.

84. (New) The memory device of claim 82 wherein the ring oscillator includes N delay stages that generate tap clock signals T1-TN, respectively, and the latch and compare circuit latches tap clock signals T1-TN from the ring oscillator and performs an XOR operation on each pair of latched tap clock signals T1-T2, T2-T3, and so on through TN-1-TN, and also performs an XOR operation on the pair T1 and TN, with each XOR operation generating a corresponding fine delay signal.

85. (New) The memory device of claim 84 wherein the fine delay transform circuit operates in a first mode responsive to a selected one of the tap clock signals T1-TN having a first logic state.

86. (New) The memory device of claim 85 wherein the fine delay transform circuit operates in a second mode responsive to a selected one of the tap clock signals T1-TN having a second logic state.